

SHEET 1 of 1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO - 1449				ATTORNEY DOCKET NO. 00791/LH			SERIAL NO. 09/704,156	
				APPLICANT: Takeshi WAKABAYASHI				
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U.S. PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB		
LT		5,155,068	10/1992	Tada				
LT		5,977,641	11/1999	Takashashi et al				
LT		5,989,982	11/1999	Yoshikazu				
FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB	TRANSLATION	
							YES	NO
LT		0 706 208	04/1996	EPO			X	
		0 853 337	07/1998	EPO			X	
		08-070081	03/1996	Japan			X*	
		11-121507	04/1999	Japan			X*	
LT		11-224980	08/1999	Japan			X*	
OTHER DOCUMENTS (AUTHOR, TITLE, DATE, PAGES, PUBLICATION, ETC.)								
LT	Masatoshi YASUNAGA et al: "CHIP SCALE PACKAGE* (CSP) A LIGHTLY DRESSED LSI CHIP", Proceedings of the IEEE/CPMT International Electronics Manufacturing Technology Symposium, New York, U.S., IEEE Vol. Symp. 16, pages 169-176 XP000530088, ISBN: 0-7803-2038-7, page 169 - page 171; Figures 1-6.							
EXAMINER: <i>Luan Thai</i>				DATE CONSIDERED: <i>1/31/02</i>				
*English language Abstract only.								

March 7, 2001

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